CLAIMS:

We claim:

1. A semiconductor memory device comprising:

a memory cell array including a plurality of word lines arranged in a row direction, a plurality of bit lines and a plurality of column selecting lines arranged in a column direction, and a plurality of memory cell array blocks arranged in the column direction;

a plurality of internal voltage generating lines arranged between the plurality of the memory cell array blocks;

a column decoder arranged on a first side of the memory cell array and configured to select one of the column selecting lines;

an internal voltage generating circuit arranged on both the first and a second side of the memory cell array and configured to compare a reference voltage to an internal voltage to generate a comparing signal; and

a plurality of drivers arranged on both ends of the plurality of internal voltage generating lines, respectively, and configured to supply the internal voltage to the plurality of internal voltage generating lines in response to the comparing signal.

2. The device of claim 1, wherein the plurality of drivers comprises:

a plurality of first drivers coupled to the plurality of the internal voltage generating lines on the first side of the memory cell array; and

a plurality of second drivers coupled to the plurality of internal voltage generating lines on the second side of the memory cell array.

3. The device of claim 2, further comprising:

a first external voltage applying pad configured to apply an external voltage to the plurality of first drivers; and

a second external voltage applying pad configured to apply the external voltage to the plurality of second drivers.

4. The device of claim 3, further comprising:

a first external voltage applying pin configured to apply the external voltage to the first external voltage applying pad; and

a second external voltage applying pin configured to apply the external voltage to the second external voltage applying pad.

5. The device of claim 2, wherein the column decoder comprises:

a column address input buffer for receiving and buffering the column address;

a column address pre-decoder for pre-decoding the buffered column address; and

a plurality of column selecting line driving circuits for driving the plurality of column selecting lines in response to the pre-decoded column address,

wherein the plurality of second drivers are arranged between the plurality of column selecting line driving circuits.

6. A device comprising:

a memory cell array having a first and a second memory cell array block;

an internal voltage generating line arranged between the first and the second memory cell array blocks;

a first and a second active internal voltage generating circuit arranged on a first and second side, respectively, of the memory cell array; and

a first and a second driver coupled to the first and the second active internal voltage generating circuits, respectively, and coupled to a first and a second end, respectively, of the internal voltage generating line.

7. The device of claim 6, further comprising:

a first external voltage pad configured to apply an external voltage to the first driver; and

a second external voltage pad configured to apply the external voltage to the second driver.

8. The device of claim 7, further comprising:

a first external voltage pin coupled to the first external voltage pad; and

a second external voltage pin coupled to the second external voltage pad, the second external voltage pin separated from the first external voltage pin.

9. A layout method of a semiconductor memory device comprising:

arranging a plurality of memory cell array blocks of a memory cell array in a column direction;

arranging a plurality of internal voltage generating lines between the plurality of memory cell array blocks;

arranging a column decoder to one side of the memory cell array;

arranging an active internal voltage generating circuit to two sides of the memory cell array; and

arranging a plurality of drivers of the active internal voltage generating circuit on two sides of the plurality of the internal voltage generating lines.

10. The method of claim 9, wherein arranging a plurality of drivers comprises:

arranging a plurality of first drivers of the active internal voltage generating circuit on one side of the plurality of the internal voltage generating lines;

arranging a plurality of second drivers of the active internal voltage generating circuit on another side of the plurality of the internal voltage generating lines; and

arranging a first external voltage applying pad for applying an external voltage to the plurality of the first drivers and a second external voltage applying pad for applying the external voltage to the plurality of the second drivers.

11. The method of claim 9, wherein a first external voltage applying pin for applying the external voltage to the first external voltage applying pad is separated from a second external voltage applying pin for applying the external voltage to the second external voltage applying pad.

12. A method comprising:

coupling a first driver from a first active internal voltage circuit to a first end of an internal voltage generating line that is structured to supply an internal voltage to a memory cell array block; and

coupling a second driver from a second active internal voltage circuit to a second end of the internal voltage generating line.

13. The method of claim 12, further comprising:

simultaneously driving the internal voltage generating line with the first driver and the second driver.

14. The method of claim 12, further comprising:

supplying an external voltage to the first driver using a first external voltage pad; and

supplying the external voltage to the second driver using a second external voltage pad.

15. The method of claim 12, wherein coupling the first driver and coupling the second driver comprises:

arranging the first driver and the second driver between two column selecting lines.